-- chip -- .

Page 23, lines 1-2 and 8, change "through hall" to -- elongate opening -- .

Page 24, lines 2, 5, 7, 9, 12 and 20 (second occurrence), change "element" to

-- chip -- .

Page 24, lines 3 and 22, change "through hall" to -- elongate opening -- .

Page 25, lines 1, 3, 5 and 8, change "element" to -- chip -- .

In the Claims

Please cancel Claims 1-6 without prejudice.

Please amend claims 10 and 11 as follows:

Claim 10, line 2, delete "8 or 9,".

Claim 11, line 2, delete "8 or 9,".

Please add new claims 12-23 as follows:

--12. A method of manufacturing a semiconductor device as claimed in claim 8, wherein the surface where the element is formed of said semiconductor element is fixed on the one side of said substrate semiconductor package via a tape-like bonding material.

13. A method of manufacturing a semiconductor device as claimed in claim 9,

wherein the surface where the element is formed of said semiconductor element is fixed on the one side of said substrate semiconductor package via a tape-like bonding material.

14. A method of manufacturing a semiconductor device as claimed in claim 8, wherein the surface where the element is formed of said semiconductor element is fixed on the one side of said substrate of said semiconductor package with adhesive.

15. A method of manufacturing a semiconductor device as claimed in claim 9, wherein the surface where the element is formed of said semiconductor element is fixed on the one side of said substrate of said semiconductor package with adhesive.

16. A semiconductor device comprising:

a substrate having a first surface and a second surface opposed to the first surface, said substrate further having an elongate opening defined therethrough from the first surface to the second surface;

a plurality of connecting patterns located on the second surface of said substrate, each of the plurality of connecting patterns having a first end;

a semiconductor chip having a surface which is mounted to the first surface of the substrate;

a plurality of electrodes located on the surface of said semiconductor chip and

aligned with said elongate opening of said substrate;

a plurality of wires extending within the elongate opening of said substrate and respectively electrically connecting said plurality of electrodes to corresponding ones of said plurality of patterns;

a resin which covers said plurality of electrodes, said plurality of wires, and the first ends of said plurality of connecting patterns; and

a solder resist which covers the side walls of the surface and the other end of said connecting patterns.

17. A semiconductor device as claimed in claim 16, wherein said substrate includes an upper plate and a lower plate which define a step configuration in the second surface of said substrate, wherein the upper plate is located between said semiconductor chip and said lower plate, and wherein the plurality of connecting patterns extend continuously from said upper plate to said lower plate such that the first end of the plurality of connecting patterns are located on said upper plate.

18. A semiconductor device comprising:

a substrate having a first surface and a second surface opposed to the first surface, said substrate further having first and second elongate openings defined therethrough from the first surface to the second surface;

a plurality of connecting patterns located on the second surface of said substrate, each of the plurality of connecting patterns having a first end;

a semiconductor chip having a surface which is mounted to the first surface of the substrate;

a plurality of electrodes located on the surface of said semiconductor chip, each of said plurality of electrodes aligned with one of said first and second elongate openings of said substrate;

a plurality of wires each extending within one of the first and second elongate openings of said substrate and respectively electrically connecting said plurality of electrodes to corresponding ones of said plurality of patterns;

a resin which covers said plurality of electrodes, said plurality of wires, and the first ends of said plurality of connecting patterns; and

a solder resist which covers the side walls of the surface and the other end of said connecting patterns.

19. A semiconductor device as claimed in claim 18, wherein said substrate includes an upper plate and a lower plate which define a step configuration in the second surface of said substrate, wherein the upper plate is located between said semiconductor chip and said lower plate, and wherein the plurality of connecting patterns extend continuously from said upper plate to said lower plate such that the first end of the

plurality of connecting patterns are located on said upper plate.

20. A semiconductor device as claimed in claim 16, wherein the elongate opening is smaller than the semiconductor chip.

21. A semiconductor device as claimed in claim 18, wherein the first and second elongate openings are smaller than the semiconductor chip.

A2 Concl'd

22. A semiconductor device according to claim 16, further comprising a bonding material formed on the entire surface of the first surface of the substrate, wherein the semiconductor chip is mounted on the first surface of the substrate via the bonding material.

23. A semiconductor device according to claim 18, further comprising a bonding material formed on the entire surface of the first surface of the substrate, wherein the semiconductor chip is mounted on the first surface of the substrate via the bonding material. --